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7. (a) Discuss multiplication Algo for signed magnitude data. Show the steps for multiplexing :

$$10011 \times 10111$$

(Multiplicand) (Multiplier)

- (b) Discuss Handshaking as a technique of Asynchronous data transfer.

8. (a) WAP in 8085 Assembly language programming for the following :

Ten bytes of Data are stored in memory location at 2050H to 2059H. Transfer entire block of data to a new memory area starting at address 2080H.

- (b) Discuss the steps in memory read operation in 8085 μ P.

9. Discuss PUSH, LDAX, LXI, RAL, INC, INX instructions with exact format, example and meaning.

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**B. C. A. (Third Semester)
EXAMINATION, Nov./Dec., 2018**

(New Course)

Paper Third

COMPUTER ARCHITECTURE AND
ASSEMBLY LANGUAGE

Time : Three Hours] [Maximum Marks : 75

Note : Attempt questions from all Sections as directed.

Inst. : The candidates are required to answer only in serial order. If there are many parts of a question, answer them in continuation.

Section—A

(Short Answer Type Questions)

Note : All questions are compulsory. Each question carries 3 marks.

1. (A) What is DMA ? Discuss in brief.
- (B) Show the memory interfacing of 8085 micro-processor with 4096×8 RAM. Show the valid address range for your design.
- (C) Discuss flag register in 8085.

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- (D) Discuss three different data transfer instruction formats in 8085 microprocessor and explain each.
- (E) Discuss different branch instructions in intel 8085 (any six) with meaning.
- (F) WAP in 8085 Assembly language to subtract 20H from 87H, where 20H is in memory location 2050H and 87H is an address 2051H. Store the result in memory location 2053H.
- (G) Discuss 1-address and 0-address instruction format to calculate $X = A + B * C$.
- (H) What is Priority interrupt and discuss any method to handle it?
- (I) Discuss Stack based CPU organization.

Section—B

(Long Answer Type Questions)

Note : Attempt any two questions. Each question carries 12 marks.

2. Define Computer architecture and Computer organization.

A digital computer has a common bus system for 16 registers of 32 bit each. The bus is constructed with multiplexer :

- (a) How many selection inputs are there in each multiplexer (MUX) ?
- (b) What size of MUXs are needed ?
- (c) How many MUXs are there in the bus ?
- Show the organization of the bus for the above.

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3. Describe the following shift microoperations in detail with example (take the initial value of R = 1101 1101) :
- (i) Logical shift (Left and Right)
- (ii) Circular shift (Left and Right)
- (iii) Arithmetic shift (Left and Right)
4. (a) Discuss different registers that are part of CPU architecture in 8085 microprocessor. (With MM size 64 K byte having word size as one byte). Specify purpose of each register with size.
- (b) Discuss instruction cycle in detail.
5. (a) Discuss program driven I/O and interrupt driven I/O.
- (b) Show a bus organized CPU organization schematically having 16 registers with 32 bit each.
- Formulate a control word for the system assuming ALU has 35 operations.

Section—C

(Long Answer Type Questions)

Note : Attempt any two questions. Each question carries 12 marks.

6. (a) Discuss pipelining. How does it increase the CPU throughput ? Show with an example.
- (b) Discuss the following pin info in intel 8085 μP with :

$\overline{ALE}$, $\overline{IO/M}$, $\overline{INTA}$, $\overline{HOLD}$

Discuss programming model of 8085 μP with size, meaning, name of CPU registers used.

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